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B. E. (Third Semester) Examination, April-May 2021

(New Scheme)

(ET&T Engg. Branch)

DIGITAL ELECTRONICS & LOGIC DESIGN

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note : *Attempt all questions. Part (a) of each unit is compulsory carrying 2 marks. Attempt any* ***two*** *parts from parts (b), (c) and (d) carrying 7 marks each.*

Unit-I

1. (a) Define self complementing code.

(b) Explain De-morgan's theorem with example.

(c) Explain Hamming code detection and correction method with suitable example.

(d) Convert the following :

(i) $(10101)_2$ to decimal

(ii) $(367{\cdot}52)_8$ to binary

(iii) $(5C7)_{16}$ to decimal

(iv) $(110101{\cdot}101010)_2$ to octal

Unit-II

2. (a) What are "don't care" combinations?

(b) Evaluate the minimal expression using Quine-McCluskey method :

$$f(A, B, C, D) = \sum m(0, 1, 3, 7, 8, 9, 11, 15)$$

(c) Evaluate the function

$$F(A, B, C, D) = \sum m(1, 5, 6, 12, 13, 14) + d(2, 4)$$

using K-map minimization technique.

(d) Describe the operation of PAL with suitable diagram.

Unit-III

3. (a) Compare a decoder with multiplexer.

(b) Define full-adder. Design a full-adder using half-adder.

(c) Design an even parity bit generator for a 4-bit input.

(d) Design 4-to-16 decoder from Two 3-to-8 decoders.

Unit-IV

4. (a) Define Sequential circuit.

(b) Design a 3 bit synchronous up-counter usig J-K flip flops.

(c) What is Shift Register? Give its types.

(d) Design a circuit than convert JK flip-flop to T-flip-flop.

Unit-V

5. (a) Define Tri-state logic.

(b) Describe Diode Transistor Logic (DTL) NAND gate with its logic operation with relevant diagram.

(c) Explain the ECL logic family. Why it is the fastest of all logic families.

(d) Compare the performance of TTL, CMOS and ECL logic.